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EXAMINER	
LUU, PHO M	

ART UNIT	PAPER NUMBER
2824	

DATE MAILED: 05/04/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/796,111	KLEIN A. DEAN	
	Examiner	Art Unit	
	Pho M. Luu	2824	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-85* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *12-61,69-73 and 81-85* is/are allowed.

6)☒ Claim(s) *1-9,62-66 and 74-78* is/are rejected.

7)☒ Claim(s) *10,11,67,68,79 and 80* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *10 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *01/31/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☒ Other: *Search History*.

DETAILED ACTION

1. This office action is supersedes the previous of date 03 November 2004.

2. This office acknowledges receipt of the following items from the Applicant:

-Amendment after non-final rejection filed 1/31/2005.

-Claims, Abstract, Applicant Argument and IDS filed on 1/31/2005.

3. Claim 1-85 are pending in the application.

Information Disclosure Statement

4. Acknowledgment is made of applicant's Information Disclosure Statement (IDS) Form PTO-1449, filed 31 January 2005. The information disclosed therein was considered.

Specification

5. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States

only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

7. Claims 1, 3-5, 7-8, 62, and 64-65 are rejected under 35 U.S.C. 102(e) as being anticipated by Shimizu et al. (US. 6,628,559).

For the purpose of this rejection, Shimizu et al in Figure 1 and 3, shown that the control circuit 2 (Fig. 1) coupled to the row decoder 4 (row decoder 4 includes row selection control circuit 1000, Figure 1, see column 6, lines 59-60 and control circuit 1000 including a refreshing control circuit 400, Figure 3, see column 8, lines 9-10) to completed the refreshing operation in memory 10000 (Figure 1, see column 8, lines 8-14) to generate to the output memory mat 6 (Figure 1) of the memory device 10000.

Regarding **independent claim 1** and **dependent claim 3**, Shimizu et al in Figure 1-3 discloses a memory refresh circuit (10000, Figure 1) comprising:

a control circuit (2, Figure 1) for conduct a memory refresh operation when the refresh operation is completed (see explain above).

With respected to **dependent claim 4**, Shimizu et al in Figure 1 disclosed a signal (circuit 14 input/output with control circuit 2 with refresh execution signal REFACT can be perform in device 10000) indicate when the refresh operation is completed.

For the purpose of this rejection, Shimizu et al in Figure 1 and 3, shown that the control circuit 2 (Fig. 1) coupled to the row decoder 4 (row decoder 4 includes row selection control circuit 1000, Figure 1, see column 6, lines 59-60 and control circuit 1000 including a refreshing control circuit 400, Figure 3, see column 8, lines 9-10) to completed the refreshing operation in memory 10000 (Figure 1, see column 8, lines

8-14) for generate the output memory mat 6 (Figure 1) of the memory device 10000.

Regarding **independent claim 5** and **dependent claim 7**, Shimizu et al in Figure 1-3 discloses a memory device (10000, Figure 1) comprising:

a memory array (7, Figure 1);

a refresh circuit (400, Figure 3) for controlling a refresh operation of the memory array (7, Figure 1) and for indicating when the refresh operation is complete (see explain above).

With respected to **dependent claim 8**, Shimizu et al in Figure 1 disclosed a signal (circuit 14 input/output with control circuit 2 with refresh execution signal REFACT can be perform in device 10000) indicate when the refresh operation is completed.

For the purpose of this rejection, Shimizu et al in Figure 1 and 3, shown that the control circuit 2 (Fig. 1) coupled to the row decoder 4 (row decoder 4 includes row selection control circuit 1000, Figure 1, see column 6, lines 59-60 and control circuit 1000 including a refreshing control circuit 400, Figure 3, see column 8, lines 9-10) to completed the refreshing operation in memory 10000 (Figure 1, see column 8, lines 8-14) for generate the output memory mat 6 (Figure 1) of the memory device 10000.

Regarding **independent claim 62** and **dependent claim 64**, **Shimizu et al** in Figure 1-3 discloses an integrated circuit comprising of the memory device (10000, Figure 1) comprising:

a memory array (7, Figure 1);

a refresh circuit (400, Figure 3) for controlling a refresh operation of the memory array (7, Figure 1) and for indicating when the refresh operation is complete (see explain above).

With respected to **dependent claim 65**, **Shimizu et al** in Figure 1 disclosed a signal (circuit 14 input/output with control circuit 2 with refresh execution signal REFACT can be perform in device 10000) indicate when the refresh operation is completed.

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claims 2, 6 and 63 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shimizu et al. (US. 6,628,559) in view of Takahashi et al. (US. 6,751,144).

Regarding claim **dependent claims 2, dependent claim 6 and dependent claim 63, Shimizu et al** discloses a memory refresh circuit such as a **independent claim 1, independent claim 5 and independent claim 62** above, with the exception of refresh circuit including a refresh counter.

Takahashi et al in Figure 1 discloses a refresh control circuit (4, Figure 1) incorporates a refresh counter (a refresh control circuit 4 including an address counter such as refresh counter, see column 13, lines 24-25).

It would have been obvious at the time the invention was made to a person having ordinary skill in the art using the refresh circuit of **Shimizu et al** including the refresh counter of **Takahashi et al**, for the purpose of perform the same refresh operation as the refresh circuit observed in semiconductor memory device (see column 13, lines 32-33).

10: Claim 9 and 66 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shimizu et al. (US. 6,628,559) in view of Tsukude et al. (US. 6,697,910).

Regarding claim **dependent claim 9 and dependent claim 66, Shimizu et al** discloses a memory device (10000, Figure 1) as in **independent claim 5, independent and claim 62** as above, with the exception of control circuit providing a first control signal to the refresh circuit and the refresh circuit providing a second control signal to the control circuit.

Tsukude et al in Figure 1 discloses a control circuit (20, Figure 1) which is including the input signal (/CE, /OE, /WE, /LB, /UB) coupled to the output (int/CE, int/RE, int/WE) of the refresh circuit (40) and refresh circuit (40) input (/REFE) to the control circuit (20).

It would have been obvious at the time the invention was made to a person having ordinary skill in the art using the refresh circuit of **Shimizu et al** including the control circuit of **Tsukude et al**, for the purpose of perform the output operation from the refresh circuit provide in the completed hidden refresh function in semiconductor device (see column 3, lines 43-47).

11. Claim 74 and 76-77 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shimizu et al. (US. 6,628,559) in view of Moazzami et al. (US. 5,270,967).

For the purpose of this rejection, Shimizu et al in Figure 1 and 3, shown that the control circuit 2 (Fig. 1) coupled to the row decoder 4 (row decoder 4 includes row selection control circuit 1000, Figure 1, see column 6, lines 59-60 and control circuit 1000 including a refreshing control circuit 400, Figure 3, see column 8, lines 9-10) to completed the refreshing operation in memory 10000 (Figure 1, see column 8, lines 8-14) for generate the output memory mat 6 (Figure 1) of the memory device 10000.

Regarding **independent claim 74** and **dependent claim 76**, **Shimizu et al** in Figure 1-3 discloses a processor system comprising:

memory device (10000, Figure 1) comprising:

a memory array (7, Figure 1);

a refresh circuit (400, Figure 3) for controlling a refresh operation of the memory array (7, Figure 1) and for indicating when the refresh operation is complete (see explain above). However, **Shimizu et al.** fail to explicitly mention a processor system comprising a processor.

Moazzami et al, for example, teaches a processor (204, Figure 6).

Therefore, it would have been obvious for one of ordinary skill in the art at the time the invention was made to modify the memory device of **Shimizu et al.** with the aforementioned teaching of **Moazzami et al**, since it is known in the art that the memory device using the processor can be programmed during a refresh operation other normal

accesses of the memory can be suspended unit the refresh operation is completed (see column 13, lines 63-66).

With respected to **dependent claim 77**, **Shimizu et al** in Figure 1 disclosed a signal (circuit 14 input/output with control circuit 2 with refresh execution signal REFACT can be perform in device 10000) indicate when the refresh operation is completed.

12. Claims 75 is rejected under 35 U.S.C. 103(a) as being unpatentable over Shimizu et al. (US. 6,628,559) in view of Moazzami et al (US. 5,270,967) and Takahashi et al. (US. 6,751,144).

Regarding claim **dependent claims 75, Shimizu et al** and **Moazzami et al** discloses a memory refresh circuit such as **independent claim 74** above, with the exception of refresh circuit including a refresh counter.

Takahashi et al in Figure 1 discloses a refresh control circuit (4, Figure 1) incorporates an refresh counter (a refresh control circuit 4 including an address counter such as refresh counter, see column 13, lines 24-25).

It would have been obvious at the time the invention was made to a person having ordinary skill in the art using the refresh circuit of **Shimizu et al** by incorporating the processor with **Moazzami et al** for the purpose of perform the same refresh operation as the refresh circuit observed in semiconductor memory device **Takahashi et al** (see column 13, lines 24-25).

13. Claims 78 is rejected under 35 U.S.C. 103(a) as being unpatentable over

Shimizu et al. (US. 6,628,559) in view of Moazzami et al (US. 5,270,967) and Tsukude et al. (US. 6,697,910).

Regarding claim **dependent claims 78, Shimizu et al** and **Moazzami et al** discloses a memory refresh circuit such as **independent claim 74** above, with the exception of control circuit providing a first control signal to the refresh circuit and the refresh circuit providing a second control signal to the control circuit.

Tsukude et al in Figure 1 discloses a control circuit (20, Figure 1) which is including the input signal (/CE, /OE, /WE, /LB, /UB) coupled to the output (int/CE, int/RE, int/WE) of the refresh circuit (40) and refresh circuit (40) input (/REFE) to the control circuit (20).

It would have been obvious at the time the invention was made to a person having ordinary skill in the art using the refresh circuit of **Shimizu et al** by incorporating the processor with **Moazzami et al** for the purpose of perform the output operation from the refresh circuit provide in the completed hidden refresh function in semiconductor device **Tsukude et al**. (see column 3, lines 43-47).

Allowable Subject Matter

14. Claims 10-11, 67-68 and 79-80 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

15. The following is a statement of reasons for the indication of allowable subject matter:

Regarding claim 10, the prior art of record do not disclose or suggest a memory device including an address multiplexer receiving control signal from the logic circuit.

Regarding claim 67, the prior art of record do not disclose or suggest a memory device including an address multiplexer receiving control signal from the logic circuit.

Regarding claim 79, the prior art of record do not disclose or suggest a memory device including an address multiplexer receiving control signal from the logic circuit.

16. Claims 12-61, 69-73 and 81-85 are allowed.

The following is an examiner's statement of reasons for allowance:

There is no teaching or suggestion in the prior art to: "a combining circuit for combining the refresh completed signals from the memory device to obtain a combined refresh complete signal" as claimed in the independent claim 12 and independent claim 24; or

"a temperature integration circuit for incorporating temperature into a refresh operation" as claimed in the independent claim 35 and independent claim 42; or

"a refresh circuitry is adapted to initiate the refresh operation partially in response to the environmental condition sense by the sensor which is indicate when the refresh operation is complete" as claimed in the independent claim 45, independent claim 69 and independent claim 81.

"a refresh completed signal when the burst self-refresh operation has been completed" as claimed in the independent claim 50; or

"a refresh complete signal form each memory device in the subset when the memory device complete the refresh operation" as claimed in the independent claim 61.

Conclusion

17. Any inquiry concerning this communication or earlier communications from the Examiner should be directed to Pho M. Luu whose telephone number is 571.272.1876. The examiner can normally be reached on M-F 8:00AM – 5:00PM.

If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's Supervisor, Richard Elms, can be reached on 571.272.1869. The official fax number for the organization where this application or proceeding is assigned is 703.872.9306 for all official communications.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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April 28, 2005.